REMARKS

Claims 1-24 were originally filed in the present application.

Claims 1-24 are pending in the present application.

Claims 1-24 were rejected in the July 11, 2005 Office Action.

No claims have been allowed.

Claims 1, 3, 5, 7, 13, 15, 17 and 19 are amended herein.

Claims 1-24 remain in the present application.

Reconsideration of the claims is respectfully requested.

In Section 1 of the July 11, 2005 Office Action, the Examiner objected to the disclosure for informalities on page 1. In response, Applicants have amended the specification to include copending application serial numbers and patent numbers as applicable. Applicants therefore respectfully submit that no new matter is added in the replacement paragraph and request favorable reconsideration and withdrawal of the objection.

Claims 1, 3, 5, 7, 13, 15, 17 and 19 are amended herein to correct typographical errors, namely the erroneous capitalization of the term "kth".

In Section 3 of the July 11, 2005 Office Action, the Examiner also objected to Claims 1-22 for identifying output signals from input detectors of the present invention as "[+1,+1]" and "[-1,-1]" and suggested identifying the output signals as "(+1,+1)" and "(-1,-1)", instead. Applicants note that usage of square brackets in the claims is consistent with their usage in the specification and respectfully decline to make the suggested amendment to the claims. Applicants respectfully request

withdrawal of the objection to the claims, or citation by the Examiner of a specific rule in 37 C.F.R. or in the MPEP in support of the objection.

In Section 4 of the July 11, 2005 Office Action, the Examiner rejected Claims 1-22 under 35 U.S.C. § 112, second paragraph as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Specifically, the Examiner asserted that the variable identifiers S, M, N, kth and ith are undefined in independent Claims 1 and 13. Applicants respectfully traverse the rejection.

With respect to variable identifiers S, M and N, Applicants refer to the preamble of Claim 1, which recites:

> 1. A demodulator for demodulating a set of S possible orthogonal modulation codes received serially as binary data, wherein each of said S possible orthogonal modulation codes comprises M binary bits representing an N-bit data symbol and wherein $M=2^N$, said demodulator comprising:...

Applicants respectfully assert that the identifiers S, M and N are, in fact, variable names that are defined in the preamble. The variable "S" is the number of possible orthogonal modulation codes in a set of codes demodulated by the demodulator being claimed. The variable "N" is the number of bits in a data symbol represented by one of the orthogonal modulation codes. The variable "M" is the number of binary bits in the data symbol and is specified as equal to 2^N.

With respect to the identifier "kth", Applicants respectfully assert that identifier "kth" is, in fact, a variable defined in the claims. For example, in Claim 1:

> ... a storage array capable of storing S Logic 00 code masks, each of said S Logic 00 code masks associated with one of said S possible orthogonal modulation codes, wherein a kth Logic 00 code mask comprises M/2 Logic 00 code mask bits,

> each of said M/2 Logic 00 code mask bits associated with a corresponding one of M/2 sequential pairs of M binary bits in a kth orthogonal modulation code, wherein said each M/2 Logic 00 code mask bit is a Logic 1 if said corresponding sequential pair of said M binary bits in said kth orthogonal modulation code is equal to a Logic 00 value and is equal to Logic 0 otherwise; ...

Thus, the variable "kth" is the number of Logic 00 code masks in an orthogonal modulation code equal to a Logic 00 value.

With respect to variable identifier "ith", it appears as if the Examiner mistakenly cited an rejection to "ith" instead of "jth". If this assumption is correct, Applicants respectfully assert that the identifier "jth" is, in fact, a variable defined in the claims. For example, in Claim 1:

> ... an input decision circuit capable of detecting a [+1,+1] signal output by said Logic 00 input detector after a comparison of a jth sequential pair of said M/2 sequential pairs of said M binary bits to a Logic 00 value and, in response to said detection, adding said [+1,+1] signal to a kth one of said S accumulators in said summation circuit if a jth one of said M/2 Logic 00 code mask bits in said kth Logic 00 code mask in said storage array is equal to Logic 1.

Thus, the variable jth is the number of sequential pairs of M/2 sequential pairs of M binary bits to a Logic 00 value.

In Claim 13, variables S, M, N, kth and jth are similarly defined as described above for Claim 1. Accordingly, Applicants respectfully request that the rejection of Claims 1-22 under §112, second paragraph, be withdrawn.

In Section 6 of the July 11, 2005 Office Action, the Examiner indicated that Claims 1-22 would be allowable if rewritten to overcome the objections and rejections under 35 U.S.C. § 112, second paragraph. Applicants thank the Examiner for this indication. Applicants have adequately addressed the above-mentioned objections and rejections and assert that Claims 1-22 are in the condition for

allowance. With respect to the Examiner's statement for reasons of allowance, Applicants will assume that the Examiner has given these claims their broadest possible construction and given the claims the full range of equivalents.

SUMMARY

For the reasons given above, Applicants respectfully request reconsideration and allowance of pending claims and that this Application be passed to issue. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this Application, Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at ***jmockler@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

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John T. Mockler
Registration No. 39,775

P.O. Drawer 800889
Dallas, Texas 75380
Phone: (972) 628-3600
Fax: (972) 628-3616
E-mail: *jmockler@davismunck.com*